IN THE SPECIFICATION

After the title, please replace "The present patent application is a Divisional of Application No. 09/289,424, filed April 9, 1999." with --The present patent application is a Divisional of Application No. 09/289,424, filed April 9, 1999, which is hereby incorporated herein by reference.--

IN THE CLAIMS

15. (Currently Amended.) A method of forming an isolated junction field effect transistor comprising:

a) depositing a layer of trench masking material on a surface of a semiconductor substrate;

b) patterning the layer of trench masking material to expose portions of the semiconductor substrate;

c) etching the semiconductor substrate to form at least ~~one~~ a first trench and a second trench, wherein each of the ~~at least one~~ first and second trenches has a bottom surface and a side surface;

d) depositing a conformal layer of spacer material;

e) forming spacers adjacent to the ~~trench~~ side surfaces of the first trench and the second trench by anisotropically etching the spacer material until the semiconductor substrate at the bottom surface of each of the ~~at least one~~ first and second trenches is exposed;

f) integrally forming a T-shaped pedestal in the semiconductor substrate by isotropically etching the exposed semiconductor substrate to form a first undercut region subjacent to the first trench and a second undercut region subjacent to the second trench, wherein a top portion of the T-shaped pedestal is disposed between the first trench and the second trench and a stem portion of the T-shaped pedestal is disposed between the first undercut region and the second undercut region;

g) filling each of the ~~at least one~~ first and second trenches with at least one dielectric material;

h) forming a gate insulator layer;

i) forming a gate electrode over the gate insulator layer; and

j) implanting impurities to form a source and a drain region.

16. (Currently Amended.) The method of Claim 15, wherein the depth of ~~the~~ each trench is substantially equal to a predetermined junction depth.

17. (Currently Amended.) The method of Claim 15, wherein the depth of ~~the~~ each trench is greater than a predetermined junction depth.

18. (Original.) The method of Claim 15, wherein the spacer layer material is a material selected from the group consisting of silicon oxide and silicon nitride.

19. (Currently Amended.) The method of Claim 15, wherein filling each of the ~~at least one~~ first and second trenches with at least one dielectric material comprises partially filling the first and second undercut regions ~~portions of the trenches~~ with an oxide of silicon such that an air gap exists adjacent the stem portion of the T-shaped pedestal.

20. (Currently Amended.) The method of Claim 15, further comprising, prior to the step of filling each of the ~~at least one~~ first and second trenches with at least one dielectric material, removing the spacers.

21. (Currently Amended.) The method of Claim 15, further comprising, prior to the step of filling each of the ~~at least one~~ first and second trenches with at least one dielectric material, thermally oxidizing inner surfaces of the ~~at least one trench~~ first and second undercut regions so as to form an oxide liner.

22. (Original.) The method of Claim 15, wherein the gate insulator comprises an oxide of silicon.

23. (Original.) The method of Claim 15, wherein the gate electrode comprises polysilicon.

24. (Original.) The method of Claim 15, wherein the source and drain regions are doped with p type ions.

25. (Original.) The method of Claim 15, wherein the source and drain regions are doped with n type ions.

26. (Currently Amended.) A method of forming an isolated junction comprising:

a) lining vertical sidewalls of a first trench and a second trench formed in a surface of a semiconductor substrate with a spacer material;

b) isotropically etching the first trench and the second trench with an etchant that is more selective for the semiconductor substrate than for the spacer material, to form ~~an undercut portion of the trench~~ a first undercut region subjacent to the first trench and a second undercut region subjacent to the second trench, wherein the first undercut region is isolated from the second undercut region by a portion of the semiconductor substrate;

c) removing the remaining spacer material;

d) oxidizing the inner surfaces of the ~~trench~~ first and second undercut regions;

e) forming air gaps in the first and second undercut ~~portion~~ regions ~~of the trench~~ by partially filling ~~trench~~ the first and second undercut regions with insulation material; and

f) implanting impurities into a portion of the semiconductor material that overlies the first and second undercut ~~portion~~ regions ~~of the trench~~.